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22850	7590	04/06/2006		EXAMINER
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314				SAXENA, AKASH
			ART UNIT	PAPER NUMBER
			2128	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/673,467	STRANG, ERIC J.
	Examiner Akash Saxena	Art Unit 2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 22 December 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-58 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-58 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 1/12/06, 12/22/05.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

1. Claim(s) 1-58 has/have been presented for examination based on amendment filed on 22nd December 2005.
2. Claim(s) 1-3, 6-7, 9, 11, 21, 28, 36, 55 and 58 are amended.
3. Previous non-final office action mailed on 22nd September 2005 is incorporated within this office action unless otherwise specified where the more current rejection for the amended claims supercedes the previous rejection.
4. The arguments submitted by the applicant have been fully considered. Claims 1-58 remain rejected. The examiner's response is as follows.

Response to Applicant's Remarks & Examiner's Withdrawals

5. Examiner withdraws the claim rejection(s) under 35 USC § 103 to claim(s) 1-58 in view of the amendments presented by the applicant. New rejections are made under 35 USC § 103 below.
6. Changes to the title are acknowledged and objection to the specification is withdrawn.

Response to Applicant's Remarks for 35 U.S.C. § 101

Applicant has argued that claim 58 - "transmission media" to be statutory under 35 USC 101 guidelines. The recent interim 101 guidelines states:

(c) Electro-Magnetic Signals

Claims that recite nothing but the physical characteristics of a form of energy, such as a frequency, voltage, or the strength of a magnetic field, define energy or magnetism, per se, and as such are nonstatutory natural phenomena. O'Reilly, 56 U.S. (15 How.) at 112-14. Moreover, it does not appear that a claim reciting a signal encoded with functional descriptive material falls within any of the categories of patentable subject matter set forth in § 101.

First, a claimed signal is clearly not a "process" under § 101 because it is not a series of steps. The other three § 101 classes of machine, compositions of matter and manufactures "relate to structural entities and can be grouped as 'product' claims in order to contrast them with process claims." 1 D. Chisum, Patents § 1.02 (1994). The three product classes have traditionally required physical structure or material.

"The term machine includes every mechanical device or combination of mechanical device or combination of mechanical powers and devices to perform some function and produce a certain effect or result." Corning v. Burden, 56 U.S. (15 How.) 252, 267 (1854). A modern definition of machine would no doubt include electronic devices which perform functions. Indeed, devices such as flip-flops and computers are referred to in computer science as sequential machines. A claimed signal has no physical structure, does not itself perform any useful, concrete and tangible result and, thus, does not fit within the definition of a machine.

A "composition of matter" "covers all compositions of two or more substances and includes all composite articles, whether they be results of chemical union, or of mechanical mixture, or whether they be gases, fluids, powders or solids." Shell Development Co. v. Watson, 149 F. Supp. 279, 280, 113 USPQ 265, 266 (D.D.C. 1957), aff'd, 252 F.2d 861, 116 USPQ 428 (D.C. Cir. 1958). A claimed signal is not matter, but a form of energy, and therefore is not a composition of matter.

The Supreme Court has read the term "manufacture" in accordance with its dictionary definition to mean "the production of articles for use from raw or prepared materials by giving to these materials new forms, qualities, properties, or combinations, whether by hand-labor or by machinery." Diamond v. Chakrabarty, 447 U.S. 303, 308, 206 USPQ 193, 196-97 (1980) (quoting American Fruit Growers, Inc. v. Brogdex Co., 283 U.S. 1, 11, 8 USPQ 131, 133 (1931), which, in turn, quotes the Century Dictionary). Other courts have applied similar definitions. See American Disappearing Bed Co. v. Arnaelsteen, 182 F. 324, 325 (9th Cir. 1910), cert. denied, 220 U.S. 622 (1911). These definitions require physical substance, which a claimed signal does not have. Congress can be presumed to be aware of an administrative or judicial interpretation of a statute and to adopt that interpretation when it re-enacts a statute without change. Lorillard v. Pons, 434 U.S. 575, 580 (1978). Thus, Congress must be presumed to have been aware of the interpretation of manufacture in American Fruit Growers when it passed the 1952 Patent Act. A manufacture is also defined as the residual class of product. 1 Chisum, § 1.02[3] (citing W. Robinson, The Law of Patents for Useful Inventions 270 (1890)).

A product is a tangible physical article or object, some form of matter, which a signal is not. That the other two product classes, machine and composition of matter, require physical matter is evidence that a manufacture was also intended to require physical matter. A signal, a form of energy, does not fall within either of the two definitions.

Based on the guidelines above, 35 USC 101 rejections are maintained for claim 58.

Response to Double Patenting

7. Applicant's arguments relating to filing a terminal disclaimer for applications 10/673,507 are considered and double patenting rejection is maintained until a terminal disclaimer is filed.

Response to Applicant's Remarks for 35 U.S.C. § 103

8. Claims 1-21, 23, 25-48, 50 and 52-58 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Chen.

Regarding Claim 1

Applicant's arguments filed 22nd December 2005 have been fully considered but they are not persuasive.

Applicant has argued new amended limitations (Remarks Pg. 16 & 17), which will be addressed later. Applicant has argued that Sonderman's model for producing theoretical semiconductor wafer is not the same as a first principle model. Examiner respectfully disagrees. There is no evidence presented that would differentiate between the model(s) provided by Sonderman, and first principle model as claimed.

Applicant has cited Sonderman Col.9 Lines 12-51 arguing that the passages are not related to first principles but have provided no explanation (Remarks Pg. 17-18).

Further, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Applicants further argue (Remarks Pg. 17 Last Paragraph) new limitations relating to computer-encoded differential equations. Please see new 35 USC 103 rejection below. It is unclear what the limitation is being argued while mentioning “generation of new manufacturing recipes” from Sonderman.

Applicants further argue (Remarks Pg. 18 ¶1) that Sonderman teaches “run to run” process feedback control. Examiner respectfully disagrees, since all the citations provided on pg.14 or remarks from the Sonderman reference do not point towards “run to run” process feedback control. Further, the amended claim language is unclear on the point being argued, i.e. “feedback correction on an actual process being performed”. Hence the arguments related to the feedback control of Sonderman not being the same as the instant application are found to be unpersuasive.

Applicants also argue (Remarks Pg. 19 ¶1st) that Sonderman (in Col.9 Lines 1-11) is teaching run-to-run limitation. This process is simply a generic feedback control process described without any temporal relation. It merely specifies how often a feedback is performed. Hence, the argument is also found to be unpersuasive.

Applicants further argue (Remarks Pg. 19 ¶2nd) that Sonderman is not teaching virtual sensor measurement. This limitation is not present in the instant application claim 1. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., virtual sensor measurement) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the

specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicants argue (Remarks Pg. 19 ¶3th onwards) relevance and application of Kee et al reference, which is neither used individually for 35 USC 102(e) nor in combination with Sonderman for 35 USC 103(a) rejection. Hence the arguments related to them are mute.

Applicants argue (Remarks Pg. 20-21) preemptively on the teachings of Jain et al. Arguments are considered mute in view that Jain et al has not been applied as yet to the claim rejection. Further, arguendo, even if Jain reference is applied, examiner disagrees with applicant that Jain et al teaches only a concept tool, as the abstract of this paper clearly states:

“Specifically, we present a mathematic-physical engine (MPE) to solve in real time, and to display three-dimensionally, the solution of sets of ordinary or partial differential equations.”

Applicant's argument against applicability of Jain reference is found to unconvincing.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 1-58 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1

Claim 1 is rejected as it discloses "first principle model describing at least one of a basic physical or chemical attributes" of semiconductor processing tool. The attributes are generically cited and indefinite making the first principle model indefinite as well.

Claims 28, 55 and 58 are rejected based on the same reason as claim 1.

Dependent claims 2-27, 29-54 and 56-57 are rejected based on their dependency on claim 1, 28 and 55 respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 1-21, 23, 25-48, 50 and 52-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article “Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena” by Jain et al (Jain hereafter).

Regarding Claim 1

Sonderman teaches a method to controlling a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17; Col.3 Lines 45-49) by inputting process data relating to an actual process being performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67; Col.7 Lines 8-20). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool describing at least one of a basic physical or chemical attributes (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation using the input data and the physical model to provide simulation results for the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5-7). Further, Sonderman teaches using the first principle simulation results to control the actual process being performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Sonderman does not explicitly teach building an empirical model and using the first principle simulation results along with the empirical model to control the process

performed by the semiconductor-processing tool. Empirical model & library as understood from the specification ([0078]) is the database of the simulation results, which provides "statistically sufficient sample of the parameter space".

Chen teaches creating an empirical model as disclosed in the specification as a statistical model built based on run-to-run or batch-to-batch results and using the results to control the process performed by the semiconductor-processing tool as well as to the next simulation step (Chen: Col.3 Lines 12-47; Col.6 Lines 34-67).

Sonderman and Chen do not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Chen to Sonderman. The motivation to combine would have been that Chen and Sonderman both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (Chen: at least in Col.3 Lines 19-23).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating

actual semiconductor modeling process (Sonderman: Fig.1; Col.7 Lines 8-20), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Regarding Claim 2

Sonderman teaches directly inputting the process data relating to the actual process being performed by the semiconductor-processing tool from at least one of physical sensor (eg. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; Col.7 Lines 8-20).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the process data relating to the actual process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator ((Sonderman: at least in Fig.1-3 Col.1; Col.4-7; Col.7 Lines 8-20)).

Regarding Claims 6-9

Sonderman teaches inputting process data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at least one of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3; Col.7 Lines 8-20).

Sonderman and Jain teach inputting fundamental equations as the set of computer encoded differential equations (Sonderman: Col.9 (equations); Jain: Pg. 372 Section V Dedicated MPE, Abstract).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claims 11-13

Sonderman teaches performing first principle simulation independent of the process performed by the semiconductor-processing tool; inputting data from to set initial & boundary condition on the first simulation model (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claim 14

Sonderman teaches using the first principles simulation result comprises using the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5 Line 56 – Col.6 Line 24).

Regarding Claims 15-19

Sonderman teaches using a network of interconnected resources to perform at least one of the process steps recited in claim 1; using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 20-21

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 23

Sonderman teaches first principle simulation controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: at least in Col 4 Lines 18-31; Col.3 Lines 45-49).

Regarding Claim 25

Sonderman teaches inputting various parameters relating to etching, deposition etc. (Sonderman: at least in Col.5 Lines 56-67)

Regarding Claim 26

Sonderman teaches inputting physical geometric data as parameters for the equipment model where the equipment could be at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: Col.5 Lines 56-67).

Regarding Claim 27

Sonderman teaches first principles simulation result controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool (Sonderman: Col.4 Lines 48-64; Fig.1-2).

Regarding Claim 28-48

System claims 28-48 disclose similar limitations as claims 1-21 and are rejected for the same reasons as claims 1-21 respectively.

Regarding Claim 50, 52-54

System claims 50 & 52-54 disclose similar limitations as claims 23 & 25-27 and are rejected for the same reasons as claims 23 & 25-27 respectively.

Regarding Claim 55

System claim 55 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 56 & 57

System claims 56 & 57 disclose similar limitations as claims 16 & 17 and are rejected for the same reasons as claims 16 & 17 respectively.

Regarding Claim 58

Article of Manufacture (computer program) claim 58 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

4. Claims 22 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article “Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena” by Jain et al (Jain hereafter), further in view of IEEE article “Heat Analysis on Insulated Metal Substrates” by Naomi Yunemura et al (Yunemura hereafter).

Regarding Claim 22

Teachings of Sonderman, Chen and Jain are disclosed in claim 1 rejection above. Sonderman also teaches that the first principle simulation models the equipment conditions, thereby modeling temperature response and pressure response during various processes (Sonderman: at least in Col.5 Lines 62-67).

Sonderman, Chen and Jain does not teach explicitly that such temperature and pressure modeling is done using ANSYS computer code. However, Jain teaches SIMD based processing to solve the computer-encoded differential equations (Jain: Pg. 370 Section III Parallel architectures for solving PDE).

Yunemura teaches that heat simulation modeling can be performed using ANSYS computer code (Yunemura: Pg. 1407 Section 1) on a silicon chip.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Yunemura to Sonderman, Chen and Jain to create a equipment model as disclosed by Sonderman. The motivation to combine would have been that Yunemura teaches heat modeling on a silicon chip affecting the thermal conductivity (Yunemura: Pg.1407 Section 2) based

on various thicknesses and Sonderman is solving the same issue for the equipment model that for example model the equipment for depositing the various layers and affects on heat and pressure. ANSYS is known in art to be used as thermal & pressure modeling tool based on finite element analysis. *Yunemura's teaching thereby facilitates computer-encoded differential equations solving which is considered to be prime issue by Jain (Jain: See Section III, Networking and Dedicated MPE's for solving the computer-encoded differential equations).*

Regarding Claim 49

System claim 49 discloses similar limitations as claim 22 and is rejected for the same reasons as claim 22.

5. Claims 24 & 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article “Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena” by Jain et al (Jain hereafter), further in view of U.S. Patent No. 6,812,045 issued to Mehrdad Nikoonahad (Nikoonahad hereafter).

Regarding Claim 24

Teachings of Sonderman, Chen and Jain are disclosed in claim 1 rejection above. Sonderman provides examples of the processing tool as etch and photolithography tools (Col.4 Lines 26-31) but does not explicitly disclose chemical vapor and physical vapor deposition system. Chen teaches fabrication equipment as Chemical Vapor Deposition (CVD) system (Col.5 Lines 1-5) but does not teach physical vapor deposition system. Jain is moot on such teachings.

Nikoonahad teaches deposition tools to include chemical vapor and physical vapor deposition system (Nikoonahad: Col.24 Lines 3-49).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Nikoonahad to Sonderman, Chen and Jain. The motivation to combine would have been that Nikoonahad and Sonderman-Chen are analogous art and both are modeling the semiconductor processing and providing feedback to the semiconductor processing tool (Sonderman: Abstract; Nikoonahad: Col.3; Col.93 Lines 20-35; Chen: Summary).

Regarding Claim 51

System claim 51 discloses similar limitations as claim 24 and is rejected for the same reasons as claim 24.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Monday, March 20, 2006



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